PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 10/701,332) Conf. No.: 5874
Filed: November 4, 2003)
Title: **A NOVEL BISR MODE TO TEST THE REDUNDANT ELEMENTS AND REGULAR FUNCTIONAL MEMORY TO AVOID TEST ESCAPES**)
Inventors: Ghasi R. Agrawal et al.)
Art Unit: 2117)
Examiner: Steve N. Nguyen)
Atty. Ref: 03-1343)

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-captioned patent application is respectfully submitted to the Honorable Board of Patent Appeals and Interferences after final rejection by Examiner Steve N. Nguyen, Group Art Unit 2117, refusing allowance of the claims as presented and amended in the above-captioned patent application. A copy of the claims in issue is included herewith in the Appendix.

The present Appeal Brief is in furtherance of the Notice of Appeal filed in this case on July 22, 2010, as well as a Notification mailed on September 15, 2010.

The Commissioner is authorized to charge payment of any additional fee required in connection with this appeal to Deposit Account No. 20-1495.

This brief contains the following items under the following headings and in the order set forth below (37 CFR 41.37):

i. Real party in interest;

ii. Related appeals and interferences;

iii. Status of claims;

iv. Status of the amendments;

v. Summary of the claimed subject matter;

vi. Grounds of rejection to be reviewed on appeal;

vii. Argument;

viii. Claims appendix;

ix. Evidence appendix; and

x. Related proceedings appendix.

The final page of this brief bears the attorney's signature.

I. REAL PARTY IN INTEREST

The real party in interest is the Assignee of the present patent application, LSI Corporation, a corporation organized and existing under the laws of the State of Delaware, having its principal place of business at 1621 Barber Lane, Milpitas, California 95035.

II. RELATED APPEALS AND INTERFERENCES

There are no other pending, related appeals or interferences known to the Appellant, Appellant's legal representative, or Assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF THE CLAIMS

Claims 1-14, 18 and 24 have been cancelled. Claims 15-17, 19-23 and 25-26 stand finally rejected and are on appeal.

IV. STATUS OF THE AMENDMENTS

The claims were amended on January 25, 2010 in response to an Office Action dated October 26, 2009. The Examiner refused to enter the amendment and issued an Advisory Action Before the Filing of an Appeal Brief on February 1, 2010. Applicant then filed a Request for Continued Examination on February 8, 2010 requesting that the Examiner consider the Response which was filed on January 25, 2010. The Examiner then issued an Office Action on February 22, 2010, maintaining his rejection of the pending claims. Applicant filed a Notice of Appeal and Pre-Appeal Brief Request for Review on July 22, 2010. The panel's decision was mailed on September 15, 2010, prompting the filing of this Appeal Brief.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention generally relates to built-in-self repair (BISR) designs, and more specifically relates to a BISR design which is configured to test redundant elements and regular functional memory to avoid test escapes.

Support for independent claim 15 can be found, among other places, at the locations indicated in parentheses:

15. A method for testing memory, said method comprising (discussed at, among other places, page 8, lines 2-3 and 13-14);

(a) performing a first test, wherein functional memory is tested (see, for example, page 8, lines 2-3; see also the top block in Figure 2);

(b) repairing the functional memory by adding access to redundant elements, thereby providing repaired functional memory (see, for example, page 8, lines 6-9; see also the third block from the top in Figure 2);

(c) performing a second test, wherein the repaired functional memory is tested (see, for example, the fourth block from the top in Figure 2);

(d) after repairing the functional memory and after testing the repaired functional memory, adding access to redundant memory not required for repair of the functional memory (see, for example, page 8, lines 10-14; see also the sixth block from the top in Figure 2); and

(e) after testing the repaired functional memory and then adding access to redundant memory not required for repair of the functional memory, performing a third test, wherein the redundant memory is tested, wherein the step of adding access to redundant memory which is not

required for the repair comprises faking defects to remap good elements with redundant elements (see, for example, page 7, lines 12-14, as well as reference numeral 106 in Figure 3).

Support for independent claim 21 can be found, among other places, at the locations indicated in parentheses:

21. A mode for testing memory, said mode comprising (discussed at, among other places, page 8, lines 1-3, 8 and 13-14);

(a) means for performing a first test, wherein functional memory is tested (see, for example, page 8, lines 2-3; see also the top block in Figure 2);

(b) repairing the functional memory by adding access to redundant elements thereby providing repaired functional memory (see, for example, page 8, lines 6-9; see also the third block from the top in Figure 2);

(c) means for performing a second test, wherein the repaired functional memory is tested (see, for example, the fourth block from the top in Figure 2);

(d) means for, after repairing the functional memory and after testing the repaired functional memory, adding access to redundant memory not required for repair of the functional memory by faking defects to remap good elements with redundant elements (see, for example, page 8, lines 10-14; see also the sixth block from the top in Figure 2); and

(e) means for, after testing the repaired functional memory and then adding access to redundant memory not required for repair of the functional memory, performing a third test, wherein the redundant memory is tested (see, for example, page 7, lines 12-14, as well as reference numeral 106 in Figure 3).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 15-17, 19-23 and 25-26 are pending in the application. Claims 1 and 5-6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent No. 6,961,881 (Frankowsky) in view of United States Patent Application Publication No. 2003/0237061 (Miller et al.) in view of United States Patent Nos. 6,661,719 (Shih) in view of United States Patent No. 6,999,357 (Tabishima).

VII. ARGUMENT

Applicant requests reconsideration of the following arguments.

Claims 15 and 21 are independent. Claim 15 specifically claims a method for testing memory which comprises the steps of performing a first test, wherein functional memory is tested; repairing the functional memory by adding access to redundant elements, thereby providing repaired functional memory; performing a second test, wherein the repaired functional memory is tested; adding access to redundant memory not required for repair of the functional memory after repairing the functional memory and after testing the repaired functional memory; and after testing the repaired functional memory and then adding access to redundant memory not required for repair of the functional memory, performing a third test, wherein the redundant memory is tested, wherein the step of adding access to redundant memory which is not required for the repair comprises faking defects to remap good elements with redundant elements. Claim 21 is similar but is directed to a mode.

Applicant respectfully asserts that none of the cited references, whether alone or in combination, disclose or suggest what is being specifically claimed in the claims of the present application. For example, none of the cited references disclose testing functional memory, repairing the functional memory by adding access to redundant elements, testing the repaired functional memory, adding access to redundant memory not required for the repair comprising faking defects to remap good elements with redundant elements, and then testing the redundant memory.

Applicant respectfully submits that there are many differences between what is being claimed and what is disclosed in the cited references, and that the Examine has used hindsight to

cherry pick from four different references to arrive at the present invention. There are many court decisions which hold that using hindsight is improper. As early as 1891, the United States Supreme Court held that:

> Knowledge after the event is always easy, and problems once solved present no difficulties, indeed, may be represented as never having had any, and expert witnesses may be brought forward to show that the new thing which seemed to have eluded the search of the world was always ready at hand and easy to be seen by a merely skillful attention. But the law has other tests of the invention than subtle conjectures of what might have been seen and yet was not. It regards a change as evidence of novelty, the acceptance and utility of change as further evidence, even as demonstration . . . Nor does it detract from its merit that it is the result of experiment and not the instant and perfect product of inventive power. A patentee may be baldly empirical, seeing nothing beyond his experiments and the result; yet if he has added a new and valuable article to the world's utilities, he is entitled to the rank and protection of an inventor . . . It is certainly not necessary that he understand or be able to state the scientific principles underlying his invention, and it is immaterial whether he can stand a successful examination as to the speculative ideas involved.

Diamond Rubber Co. v. Consolidated Rubber Tile Co., 220 U.S. 428 , 435-36.

Additionally, Applicant respectfully asserts that the Examiner has misinterpreted the references. For example, the Examiner admits that Frankowsky fails to disclose the step of adding access to redundant memory which is not required for the repair comprising faking defects to remap good elements with redundant elements, but asserts that Tanishima discloses this. Applicant respectfully traverses.

While the Examiner asserts that Tanishima et al. discloses faking defects to remap good elements with redundant elements, this is not the case. Tanishima et al. discloses replacing a **failed** memory cell array with a redundant memory cell array (see col. 6, lines 31-34 ("it is possible . . . to replace the **failed** memory cell array with the redundant memory cell array"; col. 7, lines 5-9 ("This allows the **failed** portion data written in the fuses to be transferred . . . . The

failed portion data . . . is then outputted"); and col. 8, line 4 ("without writing of the **failed** portion data")).

With regard to the sections of Tanishima et al. cited by the Examiner, namely col. 7, lines 34-37, 37-42 and 48-55, Applicant wishes to point out what is disclosed at lines 34-37 ("when testing of the redundant memory cell is performed in the testing step, **test data is fed as the failed portion data to the I/O terminals**...") and lines 48-50 ("**depending on the test data** . . . **one of the memory cell arrays is replaced** . . ."), and respectively asserts that Tanishima et al. fails to discloses adding access to redundant memory which is not required for repair, and then testing the redundant memory. In Tanishima et al., access is added because repair is or would be required.

Applicant respectfully submits that none of the references, whether alone or in combination, disclose or suggest the present invention as claimed. In view of the above amendments and remarks, Applicant respectfully requests that the present application be passed to issuance.

VIII. CLAIMS APPENDIX

15. A method for testing memory, said method comprising:

performing a first test, wherein functional memory is tested;

repairing the functional memory by adding access to redundant elements, thereby providing repaired functional memory;

performing a second test, wherein the repaired functional memory is tested;

after repairing the functional memory and after testing the repaired functional memory, adding access to redundant memory not required for repair of the functional memory; and

after testing the repaired functional memory and then adding access to redundant memory not required for repair of the functional memory, performing a third test, wherein the redundant memory is tested, wherein the step of adding access to redundant memory which is not required for the repair comprises faking defects to remap good elements with redundant elements.

16. A method as recited in claim 15, further comprising using repair information to repair the functional memory.

17. A method as recited in claim 15, wherein the step of adding access to redundant memory which is not required for the repair comprises forcing usage of redundant elements which are not needed to be used for repairing the functional memory.

19. A method as recited in claim 15, further comprising checking interaction between redundant elements of the memory which are not used and adjacent functional memory.

20. A method as recited in claim 15, wherein the step of adding access to redundant memory not required for repair of the functional memory comprises adding access to all remaining redundant memory, and wherein the step of performing a third test comprises testing all the remaining redundant memory.

21. A mode for testing memory, said mode comprising:

means for performing a first test, wherein functional memory is tested;

repairing the functional memory by adding access to redundant elements thereby providing repaired functional memory;

means for performing a second test, wherein the repaired functional memory is tested;

means for, after repairing the functional memory and after testing the repaired functional memory, adding access to redundant memory not required for repair of the functional memory by faking defects to remap good elements with redundant elements; and

means for, after testing the repaired functional memory and then adding access to redundant memory not required for repair of the functional memory, performing a third test, wherein the redundant memory is tested.

22. A mode as recited in claim 21, further comprising means for using repair information to repair the functional memory.

23. A mode as recited in claim 21, further comprising means for forcing usage of redundant elements which are not needed to be used for repairing the functional memory.

25. A mode as recited in claim 21, further comprising means for checking interaction between redundant elements of the memory which are not used and adjacent functional memory.

26. A mode as recited in claim 21, wherein the means for adding access to redundant memory not required for repair of the functional memory comprises means for adding access to all remaining redundant memory, and wherein the means for performing a third test comprises means for testing all the remaining redundant memory.

IX. EVIDENCE APPENDIX

There was no evidence presented during prosecution.

X. RELATED PROCEEDINGS APPENDIX

There are no other pending, related appeals or interferences known to the Appellant, Appellant's legal representative, or Assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

CONCLUSION

In summary, the prior art cited by the Examiner does not anticipate or render obvious the claims of the present invention because it does not disclose or suggest what is being claimed.

Therefore, Appellant respectfully requests that the Board:

1. Direct the Examiner to withdraw the rejection of claims 15-17, 19-23 and 25-26 in the application.

2. Direct the Examiner to proceed with issuance of the present application.

This Appeal Brief is respectfully submitted by:

Respectfully submitted,

Date: October 14, 2010

By: _____

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